Jennifer Lynn Dworak

Publications and Workshop Presentations

Refereed Conference and Archival Journal Publications:

[1] M. R. Grimaila, S. Lee, J. Dworak, K. M. Butler, B. Stewart, H. Balachandran, B. Houchins, V. Mathur, J. Park, L-C. Wang, and M. R. Mercer, "REDO -- Random Excitation and Deterministic Observation -- First Commercial Experiment," *Proc. 1999 IEEE VLSI Test Symposium*, Dana Point, CA., April 25 - 29, 1999, pp. 268-274. **(Best Paper Award at 1999 VLSI Test Symposium)**

[2] J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Modeling the Probability of Defect Excitation for a Commercial IC with Implications for Stuck-at Fault-Based ATPG Strategies," *Proc. 1999 International Test Conference*, Atlantic City, NJ, September 28 - 30, 1999, pp. 1031-1037.

[3] J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Enhanced DO-RE-ME Based Defect Level Prediction Using Defect Site Aggregation – MPG-D," *Proc. 2000 International Test Conference*, Atlantic City, NJ, October 3 - 5, 2000, pp. 930-939.

[4] J. Dworak, M. R. Grimaila, B. Cobb, T-C. Wang, Li-C. Wang, and M. R. Mercer "On the Superiority of DO-RE-ME / MPG-D Over Stuck-at-Based Defective Part Level Prediction," *Proceedings of the Ninth Asian Test Symposium*, Taipei, Taiwan, December 4-6, 2000, pp. 151-157.

[5] J. Dworak, J. D. Wicker, S. Lee, M. R. Grimaila, K. M. Butler, B. Stewart, L-C. Wang, and M. R. Mercer, "Defect-Oriented Testing and Defective-Part-Level Prediction," *IEEE Design and Test of Computers*, January-February, 2001, Vol. 18, No. 1, pp. 31 - 41. **(Chosen for reprinting in the Special Report Compiled by the Editors of IEEE Design and Test in 2002)**

[6] S. Lee, B. Cobb, J. Dworak, M. R. Grimaila, and M. R. Mercer, "A New ATPG Algorithm to Limit Test Set Size and Achieve Multiple Detections of All Faults." *Proceedings of the 2002 Design, Automation, and Test in Europe Conference and Exhibition*, Paris, France, March 4 - 8, 2002, pp. 94 - 99.

[7] J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Enhancing Test Efficiency for Delay Fault Testing Using Multiple-Clocked Schemes," *Proceedings of the 39th Design Automation Conference*, New Orleans, LA, June 10 - 14, 2002, pp. 371 - 374.

[8] J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Analysis of Delay Test Effectiveness with a Multiple-Clock Scheme," *Proc. 2002 International Test Conference*, Baltimore, MD, October 8 - 10, 2002, pp. 407 - 416.

[9] J. Dworak, J. Wingfield, B. Cobb, S. Lee, L.-C. Wang, and M. R. Mercer, "Fortuitous Detection and its Impact on Test Set Size Using Stuck-at and Transition Faults," *Proc. 2002 Defect and Fault Tolerance in VLSI Systems Symposium*, Vancouver, Canada, November 6 - 8, 2002., pp. 177 - 185.

[10] J. Wingfield, J. Dworak, and M.R. Mercer, "Function-Based Dynamic Compaction and its Impact on Test Set Sizes," *Proc 18th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cambridge, Massachusetts, November 3-5, 2003, pp. 167-174.

[11] J. Dworak, B. Cobb, J. Wingfield, and M.R. Mercer, "Balanced Excitation and its Effect on the Fortuitous Detection of Dynamic Defects," *Proc. of the 2004 Design, Automation, and Test in Europe Conference and Exhibition (DATE 2004)*, Paris, France, February 16-20, 2004, pp. 1066-1071. (181 papers were chosen from 702 submitted to the main technical tracks.)

[12] J. Dworak, D. Dorsey, A. Wang, and M.R. Mercer, "Excitation, Observation, and ELF-MD: Optimization Criteria for High Quality Test Sets," *Proceedings of the 2004 IEEE VLSI Test Symposium (VTS'04)*, Napa Valley, California, April 25-29, 2004, pp. 9-15**.** (**TTTC Naveena Nagi Award)**

[13] J. Dworak, J. Wingfield, and M. R. Mercer, "A Preliminary Investigation of Observation Diversity for Enhancing Fortuitous Detection of Defects," *Proc. 19th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes, France, October 11-13, 2004, pp. 460-468.

[14] V. Stojanovic, R. I. Bahar, J. Dworak, and R. Weiss, "Instruction Queue Based Transient Error Identification and Correction through Cost Effective Hardware ECC," *HPCRI: 2nd Workshop on High Performance Computing Reliability Issues*, (held in conjunction with *HPCA: Symposium on High Performance Computer Architecture)*, 2006

[15] V. Stojanovic, R. I. Bahar, J. Dworak, and R. Weiss, "A Cost-Effective Implementation of an ECC-Protected Instruction Queue for Out-of-Order Microprocessors," *Proceedings of the 43rd IEEE/ACM Design Automation Conference*, July 24-28, 2006, pp. 705-708. (~20% acceptance rate)

[16] J. Dworak, "An Analysis of Defect Detection for Weighted Random Patterns Generated with Observation/Excitation-Aware Partial Fault Targeting," *Proceedings of the 25th VLSI Test Symposium*, May 6-10, 2007 pp. 205-210. (~35% acceptance rate).

[17] J. Dworak "Which Defects Are Most Critical? Optimizing Test Sets to Minimize Failures due to Test Escapes," *Proceedings of the 2007 IEEE International Test Symposium (ITC'07)*, Santa Clara, California, October 23-25, 2007.

[18] E. Alpaslan, Y. Huang, X. Lin, W-T Cheng, and J. Dworak, "Reducing Scan Shift Power at RTL," *Proceedings of the 26th VLSI Test Symposium (VTS'08)*, pp. 139-146, April 27-May 1, 2008.

[19] Y. Shi, K. DiPalma, and J. Dworak, "Efficient Determination of Fault Criticality for Manufacturing Test Set Optimization," *Proceedings of the 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'08)*, October 1-3, 2008.

[20] K. Nepal, N. Alves, J. Dworak, and R. I. Bahar "Using Implications for Online Error Detection," *Proceedings of the 2008 IEEE International Test Conference (ITC'08)*, October 28-30, 2008. (CDROM proceedings)

[21] N. Alves, K. Nepal, J. Dworak, R. I. Bahar, "Detecting Errors using Multi-cycle Invariance Information" *2009 Design, Automation & Test in Europe Conference & Exhibition (DATE*) April 20-24, 2009 in Nice, France.

[22] N. Alves, K. Nepal, J. Dworak, and R. I. Bahar, "Compacting Test Vector Sets via Strategic Use of Implications," IEEE*/ACM International Conference on Computer Aided Design*, November 2009.

[23] E. Alpaslan, B. Kruseman, A. K. Majhi, W. Heuvalman, P. van de Wiel, and J. Dworak, "NIM- A Noise Index Model to Estimate Delay Discrepancies between Silicon and Simulation," *accepted for publication at 2010 Design, Automation & Test in Europe Conference & Exhibition (DATE*), to be held in Dresden, Germany, March 8-12, 2010.

[24] Y. Shi, W-C. Hu, and J. Dworak, "Too Many Faults, Too Little Time: On Creating Test Sets for Enhanced Detection of Highly Critical Faults and Defects" *accepted for publication at the 2010 VLSI Test Symposium* (VTS 2010), to be held in Santa Cruz California, April 18-21, 2010.

[25] N. Alves, A. Buben, K. Nepal, J. Dworak, and R. I. Bahar, "A Cost Effective Approach for Online Error Detection Using Invariant Relationships," *accepted for publication in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).*

Workshop Papers and Presentations

[26] "A Statistical Analysis of the Sensitivity to Defective Part Level Model Parameters During Test Pattern Set Selection," (with M. R. Grimaila, M. R. Mercer, J. Wicker, K. Butler, and B. Stewart), Ninth International Test Synthesis Workshop, Santa Barbara, CA, March 25-27, 2002. **(Winner of the Best Student Presentation Award at ITSW 2002)**

[27] "Using Commercial ATPG Tools to Accurately Predict and Minimize Defective Part Level," (with M. R. Grimaila, J. Wicker, K. M. Butler, B. Stewart, L-C. Wang, T. W. Williams, and M. R. Mercer), Eighth International Test Synthesis Workshop, Santa Barbara, CA, March 26 - 28, 2001.

[28] "The Effect of Uncertainty in the Model Parameter Tau on the Effectiveness of Test Sets Optimized with MPG-D," (with M.R. Grimaila, J. Wingfield, B. Cobb, S. Lee, M.R. Mercer, J. Wicker, K. Butler, B. Stewart, and B. Underwood), 3rd IEEE International Workshop on Microprocessor Test and Verification, Austin, TX, June 6-7, 2002.

[29] "A New Estimator for Mean Time to First Failure: How Bad Were Those Defective IC's We Missed?" (with D. Dorsey, A. Wang, and M. R. Mercer)," Tenth International Test Synthesis Workshop, Santa Barbara, CA, March 31-April 2, 2003.

[30] "Evaluating a Greedy ATPG Algorithm for Generating Compact Transition Test Sets in Accordance with the Principles of DO-RE-ME," (with S. Lee, B. Cobb, and M.R. Mercer), 4th International Workshop on Microprocessor Test and Verification, Austin, TX, May 29-30, 2003.

[31] "Defect Detectability Classes and their Effect on Optimal Test Pattern Generation Strategies," (with M. Ray Mercer), Eleventh International Test Synthesis Workshop, Santa Barbara, CA, April 4-7, 2004

[32] "Reducing Structural Bias: An Initial Look at Observation Diversity," (with J. Wingfield and M. Ray Mercer), 4th International Workshop on Microprocessor Test and Verification, Austin, TX, September 8-10, 2004.

[33] "A Preliminary Look at Utilizing Excitation Balance and Mandatory Assignment Identification for Defect Diagnosis," 12th International Test Synthesis Workshop, Santa Barbara, CA, April 11-13, 2005

[34] "An Investigation of Excitation Balance and Additional Mandatory Conditions for the Diagnosis of Fortuitously Detected Defects," presented at the IEEE 6th International Workshop on Microprocessor Test & Verification (MTV 2005), Austin, Texas, Nov. 3-4, 2005

[35] "Test Set Analysis for Maximization of the Time to Failure for Test Escapes," presented at the *13th International Test Synthesis Workshop,* Santa Barbara, CA, April 10-12, 2006.

[36] "An Analysis of Defect Detection and Site Observation Counts for Weighted Random Patterns and Compact Test Pattern Sets," presented at the *15th North Atlantic Test Workshop,* May 10-12, 2006.

[37] "A First Look at the Detection of Design Errors Modeled as Missing Logic as a Function of Simulation Vector Quality" (with E. Alpaslan) presented at the IEEE *7th International Workshop on Microprocessor Test & Verification* (MTV 2006), Austin, Texas, Dec. 4-5, 2006

[38] “Test Set Optimization for Minimizing Field Failure Rates due to Test Escapes,” *2007 North Atlantic Test Workshop (NATW)* held May 16-18, 2007.

[39] “Using Design Validation Input Sequences to Determine Fault Criticality for Test Set Optimization” (with Y. Shi, K. DiPalma, and W-C. Hu) presented at the *15th International Test Synthesis Workshop*, Santa Barbara, CA, April 7-9, 2008.

[40] “Detecting Multi-cycle Errors using Invariance Information,” (with N. Alves, K. Nepal, and R. I. Bahar) *IEEE European Test Symposium*, Workshop Track, May 2008.

[41] “Compacting Test Vector Sets via Strategic Use of Implications,” (with N. Alves, K. Nepal, R. I. Bahar) *International Workshop on Logic and Synthesis (IWLS),* July 2009.

[42] “Considering Functional Behavior for Probabilistic Defect Detection” (with C. Ashley-Rollman and Y. Shi) *presented at the 2009 International Test Synthesis Workshop*, March 23-25, 2009.

Other Publications:

[43] J. Dworak, D. Dorsey, A. Wang, and M. R. Mercer with IBM Technical Contact M. W. Mehalic, “Estimating Mean Time to Failure in Digital Systems Using Manufacturing Defective Part Level,” *4th Annual IBM Austin Center for Advanced Studies Conference*, Austin, TX, February 21, 2003.

[44] R. Kapur, T. W. Williams, J. Dworak, and M. R. Mercer, “Evaluating Test Compression Methods,” *International Conference on Computer Design (ICCD) Sunday Workshop with a tribute to Professor Edward J. McCluskey*, Oct. 10, 2004, San Jose, California