

Jennifer Lynn Dworak

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EDUCATION:

Texas A&M University, Ph.D. in Electrical Engineering, 2004 (GPR = 4.0)
Texas A&M University, M.S.E.E., 2000 (GPR = 4.0)
Texas A&M University, B.S.E.E., 1998 (GPR = 4.0)

PROFESSIONAL EXPERIENCE:

Assistant Professor of Engineering, Division of Engineering, Brown University, January 2005 – present
Postdoctoral Research Associate, Texas A&M University, June 2004-December 2004
Research Assistant, Texas A&M University, January 2000 – December 2000, June 2001 – August 2001,
June 2002-May 2004
Summer Engineering Intern at Schlumberger Anadrill, 1995-1998

TEACHING EXPERIENCE:

Brown University:

EN164: Design of Computing Systems, Brown University, Spring 2005
EN163: Digital Electronics Systems Design, Brown University, Fall 2005
EN292: Digital Integrated Circuit Testing, Brown University, Spring 2006
EN163: Digital Electronics Systems Design, Brown University, Fall 2006
EN52: Electrical Circuits and Signals, Brown University, Spring 2007, with Prof. Benjamin Kimia
ENGN: 2911Y: Verification, Test, Synthesis, Fall 2007
ENGN: 1640: Design of Computing Systems, Spring 2008
ENGN: 1630: Digital Electronics Systems Design, Brown University, Fall 2008
ENGN: 2912D: Networks and Network-on-Chip Design

Texas A&M

Graduate Assistant Lecturer for ELEN 248 Introduction to Digital Systems Design,
Spring 2001, Fall 2001, Spring 2002

HONORS AND AWARDS:

National and International:

National Science Foundation Graduate Research Fellowship, 2000 - 2003
Best Paper Award, VLSI Test Symposium, Dana Point, CA, 1999
Best Student Presentation Award, International Test Synthesis Workshop, March 2002
TTTC Naveena Nagi Award presented at the 2004 VLSI Test Symposium, April 2004

Local:

Awards:

Ethel Ashworth-Tsutsui Memorial Award for Research, 2002 (generally one or two female Texas A&M graduate students chosen per year)
The Association of Former Students & the Office of Graduate Studies Distinguished Graduate Student Award, Texas A&M University, 2000
Best Presentation in Section, University Undergraduate Fellow, 1997-1998

Fellowships:

Computer Engineering Fellowship for Excellent Doctoral Students in the Department of Electrical Engineering, 2003-2004
Fouraker Graduate Fellowship in the Department of Electrical Engineering, 2000
Computer Engineering Scholarship for the Retention of Outstanding Graduates in the Department of Electrical Engineering, 2000
Ebensberger Graduate Fellowship in the Department of Electrical Engineering, 1999
College of Engineering Fellowship in the Department of Electrical Engineering, 1999
Texas A&M University President's Endowed Scholarship, 1994-1998
Conrad and Marcel Schlumberger Scholarship, 1994-1998

PROFESSIONAL AND HONOR SOCIETIES AND ACTIVITIES:

Professional Society Activities:

International Test Synthesis Workshop:

Panels chair and organizing committee member for the 2006 International Test Synthesis Workshop (ITSW), Santa Barbara, California
Program chair for the 2007 International Test Synthesis Workshop (ITSW), San Antonio, Texas
Vice-General Chair for the 2008 International Test Synthesis Workshop (ITSW), Santa Barbara, California
General Chair for the 2009 International Test Synthesis Workshop (ITSW), Austin, Texas

North Atlantic Test Workshop

Program Committee Member for the 2006 North Atlantic Test Workshop (NATW), Essex Junction, Vermont
Publications Chair for the 2007 and 2008 North Atlantic Test Workshops (NATW), Boxborough, Massachusetts
Vice Program Chair for the 2009 North Atlantic Test Workshop (NATW)

Microprocessor Test and Verification Workshop (MTV)

Publications Chair for the 2005 Microprocessor Test and Verification Workshop (MTV), Austin, Texas
Finance Chair for the 2006 Microprocessor Test and Verification Workshop (MTV), Austin, Texas

Technical Program Committee Memberships:

ISQED (International Symposium on Quality Electronic Design) 2006-2008
ICCAD (International Conference on Computer-Aided Design) 2007-2008
ATS 2008 (Asian Test Symposium)
GLSVLSI 2009 (Great Lakes Symposium on VLSI)
HOST 2009 (IEEE International Workshop on Hardware-Oriented Security and Trust)

Other Activities:

Chair for the 2008 CADathlon programming competition associated with ICCAD 2008
Session Chair ICCAD 2007 (International Conference on Computer-Aided Design) and ITC 2007 (International Test Conference)
Reviewed papers for VLSI Test Symposium (VTS), ITC (International Test Conference), IEEE Design and Test of Computers, TODAES (ACM Transactions on Design Automation of Electronic Systems), TCAD (IEEE Transactions on CAD), TVLSI (IEEE Transactions on VLSI), ISQED and ICCAD

Memberships:

Institute of Electrical and Electronics Engineers (IEEE)
Association for Computing Machinery (ACM)
Tau Beta Pi Engineering Honor Society
Eta Kappa Nu Electrical Engineering Honor Society
Sigma Xi Honor Society
Phi Kappa Phi Honor Society

PUBLICATIONS:

Refereed Conference and Archival Journal Publications:

- [1] M. R. Grimaila, S. Lee, J. Dworak, K. M. Butler, B. Stewart, H. Balachandran, B. Houchins, V. Mathur, J. Park, L-C. Wang, and M. R. Mercer, "REDO -- Random Excitation and Deterministic Observation -- First Commercial Experiment," *Proc. 1999 IEEE VLSI Test Symposium*, Dana Point, CA., April 25 - 29, 1999, pp. 268-274. (**Best Paper Award at 1999 VLSI Test Symposium**)
- [2] J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Modeling the Probability of Defect Excitation for a Commercial IC with Implications for Stuck-at Fault-Based ATPG Strategies," *Proc. 1999 International Test Conference*, Atlantic City, NJ, September 28 - 30, 1999, pp. 1031-1037.
- [3] J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Enhanced DO-RE-ME Based Defect Level Prediction Using Defect Site Aggregation – MPG-D," *Proc. 2000 International Test Conference*, Atlantic City, NJ, October 3 - 5, 2000, pp. 930-939.
- [4] J. Dworak, M. R. Grimaila, B. Cobb, T-C. Wang, Li-C. Wang, and M. R. Mercer "On the Superiority of DO-RE-ME / MPG-D Over Stuck-at-Based Defective Part Level Prediction," *Proceedings of the Ninth Asian Test Symposium*, Taipei, Taiwan, December 4-6, 2000, pp. 151-157.
- [5] J. Dworak, J. D. Wicker, S. Lee, M. R. Grimaila, K. M. Butler, B. Stewart, L-C. Wang, and M. R. Mercer, "Defect-Oriented Testing and Defective-Part-Level Prediction," *IEEE Design and Test of Computers*, January-February, 2001, Vol. 18, No. 1, pp. 31 - 41. (**Chosen for reprinting in the Special Report Compiled by the Editors of IEEE Design and Test in 2002**)
- [6] S. Lee, B. Cobb, J. Dworak, M. R. Grimaila, and M. R. Mercer, "A New ATPG Algorithm to Limit Test Set Size and Achieve Multiple Detections of All Faults." *Proceedings of the 2002 Design, Automation, and Test in Europe Conference and Exhibition*, Paris, France, March 4 - 8, 2002, pp. 94 - 99.
- [7] J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Enhancing Test Efficiency for Delay Fault Testing Using Multiple-Clocked Schemes," *Proceedings of the 39th Design Automation Conference*, New Orleans, LA, June 10 - 14, 2002, pp. 371 - 374.
- [8] J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Analysis of Delay Test Effectiveness with a Multiple-Clock Scheme," *Proc. 2002 International Test Conference*, Baltimore, MD, October 8 - 10, 2002, pp. 407 - 416.
- [9] J. Dworak, J. Wingfield, B. Cobb, S. Lee, L.-C. Wang, and M. R. Mercer, "Fortuitous Detection and its Impact on Test Set Size Using Stuck-at and Transition Faults," *Proc. 2002 Defect and Fault Tolerance in VLSI Systems Symposium*, Vancouver, Canada, November 6 - 8, 2002., pp. 177 - 185.
- [10] J. Wingfield, J. Dworak, and M.R. Mercer, "Function-Based Dynamic Compaction and its Impact on Test Set Sizes," *Proc 18th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cambridge, Massachusetts, November 3-5, 2003, pp. 167-174.
- [11] J. Dworak, B. Cobb, J. Wingfield, and M.R. Mercer, "Balanced Excitation and its Effect on the Fortuitous Detection of Dynamic Defects," *Proc. of the 2004 Design, Automation, and Test in Europe Conference and Exhibition (DATE 2004)*, Paris, France, February 16-20, 2004, pp. 1066-1071. (181 papers were chosen from 702 submitted to the main technical tracks.)
- [12] J. Dworak, D. Dorsey, A. Wang, and M.R. Mercer, "Excitation, Observation, and ELF-MD: Optimization Criteria for High Quality Test Sets," *Proceedings of the 2004 IEEE VLSI Test Symposium (VTS'04)*, Napa Valley, California, April 25-29, 2004, pp. 9-15. (**TTTC Naveena Nagi Award**)

- [13] J. Dworak, J. Wingfield, and M. R. Mercer, "A Preliminary Investigation of Observation Diversity for Enhancing Fortuitous Detection of Defects," *Proc. 19th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes, France, October 11-13, 2004, pp. 460-468.
- [14] V. Stojanovic, R. I. Bahar, J. Dworak, and R. Weiss, "Instruction Queue Based Transient Error Identification and Correction through Cost Effective Hardware ECC," *HPCRI: 2nd Workshop on High Performance Computing Reliability Issues*, (held in conjunction with *HPCA: Symposium on High Performance Computer Architecture*), 2006
- [15] V. Stojanovic, R. I. Bahar, J. Dworak, and R. Weiss, "A Cost-Effective Implementation of an ECC-Protected Instruction Queue for Out-of-Order Microprocessors," *Proceedings of the 43rd IEEE/ACM Design Automation Conference*, July 24-28, 2006, pp. 705-708. (~20% acceptance rate)
- [16] J. Dworak, "An Analysis of Defect Detection for Weighted Random Patterns Generated with Observation/Excitation-Aware Partial Fault Targeting," *Proceedings of the 25th VLSI Test Symposium*, May 6-10, 2007 pp. 205-210. (~35% acceptance rate).
- [17] J. Dworak "Which Defects Are Most Critical? Optimizing Test Sets to Minimize Failures due to Test Escapes," *Proceedings of the 2007 IEEE International Test Symposium (ITC'07)*, Santa Clara, California, October 23-25, 2007.
- [18] E. Alpaslan, Y. Huang, X. Lin, W-T Cheng, and J. Dworak, "Reducing Scan Shift Power at RTL," *Proceedings of the 26th VLSI Test Symposium (VTS'08)*, pp. 139-146, April 27-May 1, 2008.
- [19] Y. Shi, K. DiPalma, and J. Dworak, "Efficient Determination of Fault Criticality for Manufacturing Test Set Optimization," *Proceedings of the 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'08)*, October 1-3, 2008.
- [20] K. Nepal, N. Alves, J. Dworak, and R. I. Bahar "Using Implications for Online Error Detection," *Proceedings of the 2008 IEEE International Test Conference (ITC'08)*, October 28-30, 2008. (CDROM proceedings)
- [21] N. Alves, K. Nepal, J. Dworak, R. I. Bahar, "Detecting Errors using Multi-cycle Invariance Information" *accepted for publication at the 2009 Design, Automation & Test in Europe Conference & Exhibition (DATE)* to be held April 20-24, 2009 in Nice, France.

OTHER PROFESSIONAL SOCIETY PRESENTATIONS:

- [22] "A Statistical Analysis of the Sensitivity to Defective Part Level Model Parameters During Test Pattern Set Selection," (with M. R. Grimaila, M. R. Mercer, J. Wicker, K. Butler, and B. Stewart), Ninth International Test Synthesis Workshop, Santa Barbara, CA, March 25-27, 2002. **(Winner of the Best Student Presentation Award at ITSW 2002)**
- [23] "Enhanced DO-RE-ME Based Defect Level Prediction Using Defect Site Aggregation – MPG-D," at the 2000 International Test Conference, Atlantic City, NJ, October 5, 2000.
- [24] "Using Commercial ATPG Tools to Accurately Predict and Minimize Defective Part Level," (with M. R. Grimaila, J. Wicker, K. M. Butler, B. Stewart, L-C. Wang, T. W. Williams, and M. R. Mercer), Eighth International Test Synthesis Workshop, Santa Barbara, CA, March 26 - 28, 2001.
- [25] "The Effect of Uncertainty in the Model Parameter Tau on the Effectiveness of Test Sets Optimized with MPG-D," (with M.R. Grimaila, J. Wingfield, B. Cobb, S. Lee, M.R. Mercer, J. Wicker, K. Butler, B. Stewart, and B. Underwood), 3rd IEEE International Workshop on Microprocessor Test and Verification, Austin, TX, June 6-7, 2002.

[26] "A New Estimator for Mean Time to First Failure: How Bad Were Those Defective IC's We Missed?" (with D. Dorsey, A. Wang, and M. R. Mercer," Tenth International Test Synthesis Workshop, Santa Barbara, CA, March 31-April 2, 2003.

[27] "Evaluating a Greedy ATPG Algorithm for Generating Compact Transition Test Sets in Accordance with the Principles of DO-RE-ME," (with S. Lee, B. Cobb, and M.R. Mercer), 4th International Workshop on Microprocessor Test and Verification, Austin, TX, May 29-30, 2003.

[28] "Defect Detectability Classes and their Effect on Optimal Test Pattern Generation Strategies," (with M. Ray Mercer), Eleventh International Test Synthesis Workshop, Santa Barbara, CA, April 4-7, 2004

[29] "Reducing Structural Bias: An Initial Look at Observation Diversity," (with J. Wingfield and M. Ray Mercer), 4th International Workshop on Microprocessor Test and Verification, Austin, TX, September 8-10, 2004.

[30] "A Preliminary Look at Utilizing Excitation Balance and Mandatory Assignment Identification for Defect Diagnosis," 12th International Test Synthesis Workshop, Santa Barbara, CA, April 11-13, 2005

[31] "An Investigation of Excitation Balance and Additional Mandatory Conditions for the Diagnosis of Fortuitously Detected Defects," to be presented at the IEEE 6th International Workshop on Microprocessor Test & Verification (MTV 2005), Austin, Texas, Nov. 3-4, 2005

[32] "Test Set Analysis for Maximization of the Time to Failure for Test Escapes," presented at the 13th *International Test Synthesis Workshop*, Santa Barbara, CA, April 10-12, 2006.

[33] J. Dworak "An Analysis of Defect Detection and Site Observation Counts for Weighted Random Patterns and Compact Test Pattern Sets," presented at the 15th *North Atlantic Test Workshop*, May 10-12, 2006.

[34] "A First Look at the Detection of Design Errors Modeled as Missing Logic as a Function of Simulation Vector Quality" (with E. Alpaslan) presented at the IEEE 7th *International Workshop on Microprocessor Test & Verification* (MTV 2006), Austin, Texas, Dec. 4-5, 2006

[35] J. Dworak, "Test Set Optimization for Minimizing Field Failure Rates due to Test Escapes," 2007 North Atlantic Test Workshop (NATW) held May 16-18, 2007.

[36] "Using Design Validation Input Sequences to Determine Fault Criticality for Test Set Optimization" (with Y. Shi, K. DiPalma, and W-C. Hu) presented at the 15th *International Test Synthesis Workshop*, Santa Barbara, CA, April 7-9, 2008.

OTHER PUBLICATIONS:

[37] J. Dworak, D. Dorsey, A. Wang, and M. R. Mercer with IBM Technical Contact M. W. Mehalic, "Estimating Mean Time to Failure in Digital Systems Using Manufacturing Defective Part Level," 4th *Annual IBM Austin Center for Advanced Studies Conference*, Austin, TX, February 21, 2003.

[38] R. Kapur, T. W. Williams, J. Dworak, and M. R. Mercer, "Evaluating Test Compression Methods," *International Conference on Computer Design (ICCD) Sunday Workshop with a tribute to Professor Edward J. McCluskey*, Oct. 10, 2004, San Jose, California

INVITED TALKS:

[39] "A Preliminary Analysis of Observability and Excitation Balance for the Manifestation of Errors during Verification and Field Operation," presented at AMD, Boxborough, MA, February 14, 2006.

[40] "Test Pattern Generation to Increase the Probability of Unmodeled Defect Detection," presented at Schlumberger, Sugar Land, Texas, March 28, 2006.

[41] "Fortuitous Detection of Untargeted Defects through Weighted Random Patterns Generated with Partial Fault Targeting" presented at the University of Connecticut, Storrs CT, November 14, 2006

[42] "An Analysis of Observation and Excitation Balance for Superior Testing, Verification, and Field Reliability," presented at Analog Devices, Wilmington, MA, February 20, 2007.

[43] "Developing a Unified Suite of Probabilistic Quality Metrics for Design Validation and Test," presented to Intel Corporation, March 2, 2007.

[44] "Test Set Optimization for Field Failure Reduction through Critical Error Targeting," presented to Intel Corporation, October 26, 2007.

[45] "Increasing Correct Field Operation through Critical Defect Detection," presented to ARCES, University of Bologna, November 15, 2007.

[46] Invited Panelist, "Top 3 Future Challenges in Digital Test," North Atlantic Test Synthesis Workshop, held May 16-18, 2007.

[47] "Optimizing Tests for Critical Functional Behavior (and other stuff going on at Brown!)" presented to Analog Devices, Wilmington, MA, August 8, 2008.

[48] Invited Talk: Hot Topic Background Session, "Overview of Test Generation and Analysis for Reducing Test Escapes," presented at the 2008 International Test Conference, October 28-30, 2008.

[49] "Determining Fault Criticality for Test Set Optimization and Enhanced Field Operation," to be presented at the University of Rhode Island, March 11, 2009.

GRANTS

Design Automation Conference Graduate Scholarship to support the project "A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification Based upon Structural Analysis of the Design and Stimulus," Awarded July 25, 2006 for one year, \$24,000. Scholarship awarded for support of Elif Alpaslan in this project under my supervision.

Equipment donation by Intel Corporation in support of projects in VLSI Computer-Aided Design. This generous gift consists of 6 workstations valued at approximately \$18,123. Received April 2006. Principal Investigator: Jennifer Dworak.

2007 Salomon Award for the project: "An Investigation of Pattern-Limited Test Sets for the Detection of Errors Caused by Random Defects, Systematic Defects, and Process Variations," Awarded December 2006 with one year of funding beginning January 2007, \$15,000. Principal Investigator: Jennifer Dworak.

Career Development Award: Award to Jennifer Dworak and Iris Bahar at Brown University to provide funding to develop a research collaboration with Prof. Cecilia Metra at the University of Bologna. June 1, 2007-December 31, 2008. \$8,685 Principal Investigators: Jennifer Dworak and Iris Bahar.

SHORT BIOGRAPHY:

Jennifer Dworak joined Brown University as an Assistant Professor in January 2005. She graduated in May 2004 with a Ph.D. in Electrical Engineering at Texas A&M University under the supervision of Prof. M. Ray Mercer. She graduated summa cum laude from Texas A&M University with a B.S.E.E. in December 1998 and graduated with her M.S.E.E. from Texas A&M University in May 2000. She received a National Science Foundation Graduate Fellowship and was co-author for a paper that won the Best Paper Award at the 1999 VLSI Test Symposium. She was also the winner of the Best Student Presentation Award at the 2002 International Test Synthesis Workshop and a winner of the 2004 TTTC Naveena Nagi Award. Her research interests include digital circuit testing and automatic test pattern generation, defective part level modeling, online error detection, design verification, and trust in integrated circuits.